REMARKS

The following remarks are fully and completely responsive to the Office Action dated November 17, 2004. Claims 1-5 are pending in this application. In the outstanding Office Action, claims 1-5 were rejected under 35 U.S.C. § 103(a). No new matter has been added. Claims 1-5 are presented for reconsideration.

35 U.S.C. § 103(a)

Claims 1-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' admitted prior art shown in Figure 3 (APA Figure 3) in view of Onodera (U.S. Patent No. 5,708,356). In making this rejection, the Office Action asserts that the combination of these two references teaches and/or suggests the claimed invention. The Office Action also asserts that one of ordinary skill in the art would combine these two references. Applicants disagree and request reconsideration of this rejection.

Claim 1 recites, in part:

> ...a voltage detection circuit for detecting a voltage appearing between an input side and an output side of the output transistor;
>
> a multiplying circuit for multiplying an output of the current detection circuit and an output of the voltage detection circuit together; and
>
> a protection circuit for restricting a wattage power of the output transistor according to an output of the multiplying circuit.

Onodera teaches a control circuit for supplying stabilized power to a load having voltage-current characteristics exhibiting partial negative resistance. As a result of the partial negative resistance of the load, a voltage control circuit having negative feedback

cannot be effectively used to control the voltage in the region exhibiting the negative resistance. Accordingly, Onodera teaches a control circuit that switches between negative feedback control and feed forward control. The selection of the particular control method is based on multiplying the output of a voltage variation detecting element 18 and a current variation detecting element 20.

As an initial matter, a person of ordinary skill in the art would not combine Onodera with the APA Figure 3 because Onodera's control circuit is specifically designed to deal with loads having a partial negative resistance. In contrast, neither the current invention nor the APA is designed to accommodate loads having a partial negative resistance. Accordingly, there would be no motivation to combine the control circuit of Onodera with the circuit shown in the APA Figure 3.

Furthermore, even if combined (Applicants continue to assert that one of ordinary skill in the art would not combine these two references), the combination of these two references fails to teach and/or suggest the claimed invention as discussed below.

The Office Action admits that the APA Figure 3 fails to disclose the recited voltage detection and multiplier circuits. Applicants note that since the Examiner has admitted that the APA Figure 3 does not disclose a voltage detection circuit and a multiplier circuit, the APA Figure 3 cannot teach the recited protection circuit, since the APA cannot calculate the wattage power of the output transistor.

The Office Action asserts that Onodera teaches that it is well known to use a multiplying circuit to multiply a voltage signal and a current signal, derived from voltage

and current detection circuits in order to derive a power calculation to thereby stabilize the circuit.

In contrast, Onodera teaches connecting a voltage division point p, located between the output voltage dividing resistors R1 and R2, to a voltage variation detecting element 18. The voltage variation detecting element 18 detects variations in the voltage of the voltage division point p. The voltage variation detecting element 18 is connected to a multiplier 19 (Onodera, column 3, lines 5-9).

A current detector 14 is connected to a current variation detecting element 20. The current variation detecting element 20 detects variations in the current flowing across the body electrode B. The current variation detecting element 20 is also connected to multiplier 19 (Onodera, column 3, lines 10-15).

Each of the voltage variation detecting element 18 and the current variation detecting element 20 outputs a +1-volt signal if the variation of the inputted signal is positive (i.e., either the voltage or current is increasing) and a 0-volt signal if the variation in the inputted signal is negative (i.e., either the voltage or current is decreasing).

Consequently, the output of the voltage variation detecting element 18 does not represent the voltage detected at voltage division point p. Similarly, the output of the current variation detecting element 20 does not represent the current detected at current detector 14. Consequently, the output of multiplier 19 is not, and cannot be, representative of the wattage power of the output transistor.

Consequently, even if combined (Applicants assert that one of ordinary skill in the art would not combine these two references), these two references fail to teach or

suggest at least a protection circuit for restricting a wattage power at the output transistor. These two references also fail to teach or suggest a voltage detection circuit for detecting a voltage appearing between an input side and an output side of the output transistor.

Therefore, the rejection of claims 1-5 under 35 U.S.C. § 103(a) is improper. Specifically, a person of ordinary skill in the art would not be motivated to combine the APA Figure 3 with Onodera. Furthermore, even if combined (Applicants assert that one of ordinary skill in the art would not combine these two references), these two references fail to teach and/or suggest at least a protection circuit for restricting a wattage power of the output transistor according to an output of the multiplying circuit. The combination of these two references also fails to teach and/or suggest a voltage detection circuit for detecting a voltage appearing between an input side and an output side of the output transistor. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-5 under 35 U.S.C. § 103(a).

Conclusion

Applicants' remarks have overcome the rejection set forth in the Office Action dated November 17, 2004. Specifically, Applicants' remarks have established that a person of ordinary skill in the art would not combine the APA Figure 3 with Onodera and thus overcome the rejection of claims 1-5 under 35 U.S.C. § 103(a). Even if combined, (Applicants continue to assert that a person of ordinary skill in the art would not combine these two references), the combination of these two references fails to teach and/or suggest the claimed invention. Accordingly, Applicants respectfully request

reconsideration and withdrawal of the rejection of claims 1-5 under 35 U.S.C. § 103(a). Accordingly, claims 1-5 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1-5.

Applicants submit that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 103213-00063.

Respectfully submitted,
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